28th Annual
Advanced Metallization Conference
October 4-6, 2011 • San Diego, CA

Agenda

Tuesday, October 4, 2011

8:00 AM – 8:30 AM	Registration and Continental Breakfast	
8:30 AM – 8:45 AM	Opening Remarks	

Session 1: Conference Keynote
Session Chairs: Paul Besser, Reiner Dauskardt

8:45 AM – 9:30 AM	Ultra High-Density 3D Memory Products	***R. Patti, Tezzaron Semiconductor Corp.***

Session 2: Memory Devices and Silicides
Session Chairs: Paul Besser, Reiner Dauskardt

9:30 AM – 9:55 AM	RRAM Materials and Integration *(Invited)*	***J. Kittl, IMEC***
9:55 AM – 10:15 AM	Selective CVD Tungsten as a Word Line for 3D NAND Flash Memory Application	***S. Whang, Hynix***
10:15 AM – 10:35 AM	Leakage and Contact Resistance Reduction by Diffusion of Dopants in NiPt Silicide	***A. Ozcan, IBM***
10:35 AM – 11:05 AM	Break	

Session 3: Metal Gate and High K
Session Chairs: Chia-Hong Jan, Steve Russell

11:05 AM – 11:30 AM	The Materials and Integration Challenge in Implementing & Scaling High-k/Metal Gate Transistors for High Performance CMOS *(Invited)*	***M. Chudzik, IBM***
11:30 AM – 11:50 AM	Improved 28-nm Gate Firs CMOS Transistor Engineering with a Variable Stoichiometry TiN Metal Gate	***P. Caubet, STMicroelectronics***
11:50 AM – 12:10 PM	N-Work Function Tuning Metal Layer Study for Gate-Last High-k/Metal Gate	***H. Huang, UMC***
12:10 PM – 12:35 PM	The Materials and Process Integration Challenges for iL/HiK/MG Gate Stack *(Invited)*	***S. Hung, Applied Materials***
12:35 PM – 1:55 PM	Lunch + Poster Set-up	

1:55 PM – 2:00 PM	Conference Logistics and Announcements	

Session 4: Emerging Technologies
Session Chairs: Takayuki Ohba, Heinrich Korner

2:00 PM – 2:25 PM	Performance Limitation of Cu/low-k Interconnects and Possible Future Alternatives: CNT, 3-D and Optics *(Invited)*	***K. Saraswat, Stanford***
2:25 PM – 2:45 PM	A Study on electrical resistance of CNTs and their Metal Contacts Using Simplified Test Structure	***T. Saito, LEAP***
2:45 PM – 3:10 PM	Material Characterization of Graphene *(Invited)*	***A. Toriumi, The University of Tokyo***
3:10 PM – 3:40 PM	Break	
3:40 PM – 4:00 PM	RF MEMS Planar Solenoidal Inductor with Wide Tunability	***A. Shirane, Tokyo Institute of Technology***
4:00 PM – 4:25 PM	Integrated Magnetic Inductors *(Invited)*	***P. Fischer, Intel***

ADMETA

4:25 PM – 4:40 PM	Review of ADMETA 2011 Conference Topics	***K. Ueno, Chair, ADMETA2011***

Session 5: Reception and Poster Session
Session Chairs: Roey Shaviv, Mehul Naik

4:45 PM – 6:00 PM	Reception and Poster Session	

Wednesday, October 5, 2011

8:00 AM – 8:30 AM	Continental Breakfast	
8:30 AM – 8:40 AM	Conference Logistics and Announcements	

Session 6: Copper Barriers and Metallization
Session Chairs: John Ekerdt, Eric Eisenbraun

8:40 AM – 9:05 AM	Integration Aspects of Cu-Metallization for More Than Moore Applications *(Invited)*	***W. Robl, Infineon Technologies Regensburg***
9:05 AM – 9:25 AM	Mn-Dopant Segregation as an Indicator of Barrier Integrity in 32nm Groundrule Cu/Ultra-Low K Interconnects	***A. Simon, IBM***
9:25 AM – 9:50 AM	Molecular Layer Deposition of Nanoscale Organic Films for Copper Diffusion Barriers *(Invited)*	***S. Bent, Stanford***
9:50 AM – 10:10 AM	Formation Mechanism and Suppression Methods of Copper Dendrites in BEOL Integration	***S. Yao, IBM***

10:10 AM – 10:40 AM	Break	
10:40 AM – 11:05 AM	CVD Ru Technology – Solving the Integration Challenges *(Invited)*	***T. Ishizaka, Tokyo Electron***
11:05 AM – 11:25 AM	Reflow of Copper on Ruthenium	***C. Yang, IBM***
11:25 AM – 11:45 AM	Comparison of PVD, PECVD and PEALD Ru-TaN Films with High Ru Concentration for Direct Cu Plating	***H. Wojcik, Institute for Semiconductor and Microsystems Technology, Technical University of Dresden***
11:45 AM – 12:05 PM	Enhancement of ECD Cu Fill in Extremely Narrow Trench	***J. Hong, Samsung***
12:05 PM – 12:25 PM	Ru and Pt Films Fabrication for 3D Capacitor Electrodes Using Supercritical Fluid Deposition Technique	***Y. Shimogaki, The University of Tokyo***
12:30 PM – 1:55 PM	Lunch	
1:55 PM – 2:00 PM	Conference Logistics and Announcements	
2:00 PM – 2:20 PM	Tungsten as an Alternate Conductor to Copper: Surface Scattering and the Electron Mean Free Path for (1 1 0) Epitaxial W Films	***D. Choi, Carnegie Mellon University***

Session 7: Low K Dielectrics
Session Chairs: Cindy Goldberg, Andrew McKerrow

2:20 PM – 2:45 PM	Designing Porous Ultra Low-k Dielectrics to Meet Scaling Challenges *(Invited)*	***T. Ryan, GLOBALFOUNDRIES***
2:45 PM – 3:05 PM	New Classes of ULK Dielectrics with Superior Thermomechanical Properties	***Y. Matsuda, Stanford***
3:05 PM – 3:25 PM	Integrated Capping in ULK for C028 Reliability Enhancement	***G. Imbert, STMicroelectronics***
3:30 PM – 4:00 PM	Break	

Session 8: Interconnect Reliability
Session Chairs: Christine Hau-Riege, Daniel Edelstein

4:00 PM – 4:20 PM	Effects of Al and Mn Impurities on Cu Electromigration	***C. Hu, IBM***
4:20 PM – 4:40 PM	Interpretation of Cu/SOG Stress Induced Voiding Using Stress Measurements Performed with Synchrotron Radiation	***C. Wilson, IMEC***
4:40 PM – 5:00 PM	Electromigration of Cu Interconnects Under A C, Pulsed-DC and DC Test Conditions - Practical Implications to Real Life Reliability	***R. Shaviv, Novellus Systems***

5:00 PM – 5:20 PM	Dynamic and Constant Applied Field Experiments to Characterize Dielectric Breakdown in Low-k Materials	***J. Plawsky, RPI***
5:20 PM – 5:40 PM	Size Effect on Electron Wind Force in Nano-Metallizations	***Z. Wu, UT Austin***

Thursday, October 6, 2011

8:00 AM – 8:30 AM	Continental Breakfast	
8:30 AM – 8:35 AM	Conference Logistics and Announcements	

Session 9: 3D Integration and Characterization
Session Chairs: Zsolt Tokei, Stefan E. Schulz

8:35 AM – 9:00 AM	Multi-Scale Materials Characterization for 3D IC Integration – Input for Stress Simulation and Model Validation *(Invited)*	***E. Zschech, Fraunhofer Institute for Non-Destructive Testing; Fraunhofer IZFP Dresden, Germany***
9:00 AM – 9:20 AM	Comprehensive Study of Local Strain Structures with High Strain Resolution for Through-Silicon Via Interconnects	***O. Nakatsuka, Nagoya University***
9:20 AM – 9:40 AM	Barrier Surface Pretreatment for Efficient Seed Layer Deposition in High Aspect Ratio Through Silicon Via (TSV)	***J. Cuzzocrea, STMicroelectronics***
9:40 AM – 10:05 AM	Investigation of the Mechanical Integrity of BEOL Layer Stacks with Respect to Chip-Package Interaction using BABSI Tests *(Invited)*	***H. Geisler, GLOBALFOUNDRIES Dresden Module One LLC & Co. KG***
10:05 AM – 10:30 AM	Mechanical Microprobing of Cu Pillars and Influence of Dielectric Properties on Chip-Package Interaction	***A. Hsing, Stanford***
10:30 AM – 11:00 AM	Break	

Session 10: Advanced Packaging
Session Chairs: Rajiv Joshi, Francesca Iacopi, GLOBALFOUNDRIES

11:00 AM – 11:25 AM	Thermomechanical Reliability of TSV Structures in 3D Interconnects: A Material and Design Perspective *(Invited)*	***P. Ho, UT Austin***
11:25 AM – 11:45 AM	Novel TSV Leakage Current Evaluation Using IR-Optical Beam Irradiation	***Y. Mizushima, Fujitsu***
11:45 AM – 12:10 PM	Thermal Concerns in Today's Package Interconnects *(Invited)*	***K. Tu, UCLA***
12:10 PM – 12:30 PM	Fine Pitch Cu Pillar Microbump Technology for 3D IC Integration	***S. Kim, Samsung***
12:30 PM – 12:35 PM	Wrap-up Comments from Meeting Chairs	

2011 Poster List

1	Hideki Kitada	Fujitsu	Surface Microroughness-Induced Leakage Current in Through-Silicon Via Interconnects
2	S.C. Liao	The University of Tokyo	12 Inch Bumpless Wafer-On-Wafer (WOW) Fully Integrated 3DIC Process
3	Mitsuhiro Watanabe	Fujikura	Conformal Copper Coating of True 3D Through-Holes Using Supercritical Carbon Dioxide
4	John G. Ekerdt	Cockrell School of Engineering	Chemical Vapor Deposition of Low Carbon Ruthenium-Phosphorus Alloy Films for Cu Interconnect Applications
5	Hua Ai	Applied Materials	Radical-Enhanced ALD TiN Barrier for the Burried Word-Lline (bWL) Application
6	Lawrence Hsieh	UMC	Development of a Production Worthy Dual Wafer Cu CMP Process for Direct Polishing ULK Dielectric Cu Interconnects at 28nm Technology Node
7	Paul Haumesser	CEA	All-Wet Sequence for the Metallization of Solar Cells
8	Paul Haumesser	CEA	Kinetically Size Controlled Bimetallic Nanoparticles Generated in Situ in Imidazolium Based Ionic Liquids
9	Masayuki Katgiri	LEAP	Fabrication and Characterization of Planarized Carbon Nanotube Via Interconnects
10	Holger Fiedler	Chemnitz University of Technology	Fabrication and Characterization of CNT Via Interconnects for Application in ULSI Circuits
11	Lucas Petersen Barbosa Lima	School of Electrical and Computer Engineering, University of Campinas	XPS Analyses and Work Function Extraction of Titanium Nitride Electrodes for MOS Technology and Schoktty Diode
12	Brad Bittel	Penn State	Electron Spin Resonance Studies of Interlayer Dielectrics

13	Mihoko Hirai	Consortium for Advanced Semiconductor Materials and Related Technologies (CASMAT)	Integration of an Organic Ultra Low-k Material (k=2.2) and Applying a Plasma Damage Recovery Process
14	Huai Huang	University of Texas at Austin	Effect of Fluorocarbon Plasma Chemistry on Surface Roughening of Porous OSG Low-k Films
15	Ockyoum Jeon	Samsung	Robust and Scalable p-SiOCH (k-2.2, 2.4) Films by Self-Assembly SOG (spin on glass)
16	Pavel Livshits	Bar Ilan University	The Precipitation of Gold Nanoparticles Serving as Catalyst on Insulating Substrates for Metallic Ultra-Thin Film Deposit
-	Pavel Livshits	Bar Ilan University	Thin Silver Films Electroless Deposition on Gold Nanoparticles Catalyst for Micro and Nanoelectronics
17	Kwangseon Jin	Sejong University	Atomic Layer Deposition of Copper Seed Layer for Electroplating Using Cu(dmamb)2 and H2
18	Pavel Livshits	Bar Ilan University	Nanoparticles and Plasmon Resonance Based Probe for Failure Analysis of ULSI Microchips and Electrical Characterizations of Metallic Interconnects
19	Ming-yen Li	UMC	Effect of CESL Stressors on Morphological Stability of Pt-Dissolved $NiSi_{1-x}Ge_x$ Formed on $Si_{0.72}Ge_{0.28}$ Epilayer
20	Inka Richter	GLOBALFOUNDRIES	Investigation and Monitoring of Stress Induced Voids in Ni(Pt)-Silicides
21	Olivia Huang	UMC	The Effect of B2H6-Reduced Tungsten Nucleation Layer on Contact W Corrosion