ADMETA 2006 PROGRAM

Advanced Metallization Conference 2006: 16th Asian Session

Conference: Sep. 26-27, 2006 Sanjo Conference Hall, The Univ. of Tokyo, Tokyo

[Sep. 26, 2006]

Session 1 **Opening Session** Chairperson: T. Yoda

9:50 – 10:00 Opening Remarks, A. Osaki, Chair of Asian Session [Renesas Corp.]
Award Ceremony

10:00 – 10:30(**1-1**) **Keynotes:** Tsukuba Semiconductor Consortium [Selete] H. Watanabe

10:30 – 11:00(**1-2**) **Keynotes:** [IBM] B.M. Credie

Session 2 **Low-k (1)** Chairperson: Y. Shimogaki

11:00 – 11:25(**2-1**) **Invited:** Low-k Interconnect using self-assembled porous-silica film [MIRAI] S. Chikaki

11:25 – 11:45(**2-2**) Photo-stimulated Desorption from Porous Low-k Films by UV Cure Treatments with Various Wavelength [System Devices Research Laboratories, NEC Corp.] F. Ito, T. Takeuchi and Y. Hayashi

11:45 – 12: 05(**2-3**) Mechanical and Dielectric Properties of Pure-Silica-Zeolites Low-k Materials [Univ. of California, Riverside, *California Institute of Technology, **Advanced Micro Devices Inc., ***Rice Univ., ****Teradyne Inc.] Z. Li, Y. Yan, M. Sun, C. Lew, S. Li, M. Johnson, J. Wang, M. Davis*, T. Ryan**, J. Martin**, D. Earl***, M. Deem*** and W. Maichen****

12:05 – 12:25(**2-4**) Impact of Direct CMP on surface and bulk properties of high porosity low-k dielectrics [IMEC, *Intel Corp.] N. Heylen, F. Sinapi, Y. Travaly, G. Vereecke, M. Baklanov, L. Carbonell, J. Van Hoeymissen, D. Hellin, J.L. Hernandèz, G. Beyer and P. Fischer*

12:25 – 13:15 **Lunch**

Session 3 **Metallization** Chairperson: J. Koike, M.B. Takeyama

13:15 – 13:40(**3-1**) **Invited:** Issues & potential solutions for future of interconnect technology [IMEC] S.H. Brongersma

13:40 – 14:00(**3-2**) Novel PVD process of barrier metal for Cu interconnects extendable to 45nm node and beyond [Fujitsu Ltd., *Fujitsu Laboratories Ltd.] H. Sakai, N. Shimizu*, N. Ohtsuka*, T. Tabira*, T. Kouno, M. Nakaishi and M. Miyajima

14:00 – 14:20(**3-3**) PEALD of Ru layer on WNC ALD barrier for Cu/porous low-k integration [Semiconductor Leading Edge Technologies, Inc., *ASM Japan K. K., **ASM Microchemistry, ***Ebara Corp.] K. Namba, T. Ishigami, M. Enomoto, S. Kondo, H. Shinriki*, D. Jeong*, A. Shimizu*, N. Saitoh*, W-M. Li**, S. Yamamoto***, T. Kawasaki***, T. Nakada*** and N. Kobayashi

14:20 – 14:40(**3-4**) Cu diffusion barrier property improvement of Ru by Al stuffing for future highly reliable interconnect [Dept. of Materials Engineering, The Univ. of Tokyo] A. Seki, H. Kim and Y. Shimogaki

14:40 – 15:00(**3-5**) Kinetics and Narrow-Gap Filling in Cu Thin Film Deposition from Supercritical Carbon Dioxide Fluids-Precise and Reliable Experiments using a Flow-Type Deposition Processor [Dept. of Mechanical System Engineering, Interdisciplinary Graduate School of Medicine and Engineering, Univ. of Yamanashi] E. Kondoh, M. Hirose and J. Fukuda

15:00 – 15:20(**3-6**) Reaction mechanism of low-temperature damageless cleaning of Cu_2O by HCOOH [School of Engineering, The Univ. of Tokyo, *Electronic Devices Business Group, Fujitsu Ltd., **Division of Univ. Corporate Relations, The Univ... of Tokyo] M. Sugiyama1, K. Ishikawa*, M. Nakaishi*, K. Yamashita and T. Ohba**

15:20 – 15:40(**3-7**) Copper nanoscale cluster deposition technology for ULSI interconnects [Nano Cluster Devices Ltd, *Nanostructure Engineering Science and Technology (NEST) group and MacDiarmid Institute of Advanced Materials and Nanotechnology, **Dept. of Electrical and Computer Engineering, ***Dept. of Physics and Astronomy] K.C. Tee*,**, A. Lassesson, J. van Lith, S. A. Brown*,***, R. J. Blaikie*,** and J. G. Partridge*,***

15:40 – 16:00 **Coffee Break**

Session 4 Reliability Chairperson: N. Shimizu

16:00 – 16:25**(4-1)** **Invited:** Interaction of Microstructure with Electron Wind Force [Nangyang Technological Univ.] S. Mhaisalkar

16:25 – 16:45**(4-2)** Electroless CoWP Capping for Cu/Low-k Integration [Semiconductor Leading Edge Technologies, Inc., *Ebara Corp.] T. Ishigami, T. Ishibashi*, X. Wang*, H. Ono*, A. Owatari*, S. Kondo and N. Kobayashi

16:45 – 17:05**(4-3)** Reliability Improvement and its Mechanism for Cu Interconnects with Cu-Al Alloy Seeds [Renesas Technology Corp., *Renesas Semiconductor Engineering Corp.] K. Mori, K. Maekawa, N. Amou*, D. Kodama, H. Miyazaki, N. Suzumura, K. Honda, Y. Hirose, K. Asai and M. Yoneda

17:05 – 17:25**(4-4)** Infusion Processing for Reliable Copper Interconnects [Semiconductor Leading Edge Technologies, *Epion Corp.] S. Kondo, T. Ishigami, M. Enomoto, S. Sherman*, M. Tabat* and J. Hautala*

17:25 – 17:45**(4-5)** **Guest Paper from USA**

17:50 – 20:00 Poster Exhibitor and Banquet

<Low-k>

(5-1) Mechanically Strong Ultralow-k Nanoporous Silica Made of SiOx Nanoparticles [Dept. of Electronic Engineering, UEC] S. Nozaki, H. Ono and K. Uchida

(5-2) Structural engineering of porous PE-CVD SiOC film (k<2.4) with high RIE plasma resistance [Process and Manufacturing Engineering Center, Semiconductor Company, Toshiba Corp., *Semiconductor Technology Development Group, Semiconductor Business Unit, Sony Corp.] H. Masuda, H. Miyajima, T. Idaka, T. Shimayama*, T. Kameshima*, Y. Kagawa*, T. Hasegawa*, H. Yano and T. Yoda

(5-3) Computational Approach to Structures, Properties, and Ultraviolet-cure Mechanism [Computational Materials Science Center, National Institute for Materials Science, *Collabolative Research Center for Frontier Simulation Software for Industrial Science, Institute of Industrial Science, Univ. of Tokyo, **Semiconductor Leading Edge Technologies, Inc.] J. Ushio, T. Hamada*, T. Ohno*, S. Nakao**, K. Yoneda**, M. Kato** and N. Kobayashi**

<Metallization>

(5-4) W-CVD using biscyclopentadienyltungsten system [Meiji Univ., School of Science and Technology, *Tri Chemical Laboratories Inc, **Toyota Technological Institute] S. Imai, T. Kagawa, H. Kurozaki, A. Ogura, M. Ishikawa*, I. Muramoto*, H. Machida* and Y. Ohshita**

(5-5) Ultra thin 1 nm-thick continuous PEALD-Ru formation for masking bottom barrier metal from etching solvent in wet phase and oxidation in gas phase [ASM Japan] D. Jeong, O. Souki, I. Hiroaki, A. Shimizu and H. Shinriki

(5-6) Characterization of Cu Electroplating Film on Alloy Seed Layer [Process Technology Development Division, Production and Technology Unit, Renesas Technology Corp.] S. Muranaka, M. Sueyoshi, K. Honda, Y. Hirose, S. Fukui and I. Kanno

(5-7) Nanoscale investigation of long-term native oxidation of Cu thin films [Institute of Multidisciplinary Research for Advanced Materials, Tohoku Univ., *The Key Laboratory of Automobile Materials of Ministry of Education and Dept. of Materials Science & Engineering, Jilin Univ..., **Measurement & Analysis Team, National NanoFab Center] J-W Lim, J. Iijima, Y. Zhu*, J.H Yoo**, K. Mimura, M. Isshikia

(5-8) Controlling the resistivity of fine line Cu interconnects [Dept. of Materials Science and Engineering, Ibaraki Univ., *Dept. of Electronics and Information System, Faculty of System Science and Technology, Akita Prefectural Univ., **Hitachi Research Laboratory, Hitachi Ltd., Hitachi, ***Hitachi Kyowa Engineering Ltd., Hitachi, ****Micro Device Division, Hitachi Ltd.] K. Khoo, J. Onuki, T. Nagano, Y. Chonan*, H. Akahoshi**, T. Tobita***, M. Chiba***, T. Saito**** and K. Ishikawa****

(5-9) Cu resistivity in narrow lines: grain boundary contribution control through ECD electrolyte [CEA-LETI D2NT, * ST Microelectronics] S. Maîtrejean, T. Mourier, P. Chausse, V. Safraoui*, M. Cordeau, J. Torres*, G. Passemard*

(5-10) Effect of IrOx crystal orientation on the thermal stability of Pt/IrOx bottom electrode for FeRAM capacitors [Semiconductor R&D Division, Semiconductor Business Group, Oki Electric Industry Co., Ltd.] D. Inomata, K. Abe and Y. Igarashi

(5-11) Preparation of HfNx barrier with low resistivity by using hot-wire method [Dept. of Electrical and Electronic Engineering, Kitami Institute of Technology] M.B. Takeyama, M. Sato, M. Yashiki and A. Noya

(5-12) Interface morphology in Cu/ZrN/SiOC/Si system induced by annealing [Dept. of Electrical and Electronic Engineering, Kitami Institute of Technology] M.B. Takeyama, M. Sato and A. Noya

(5-13) Comparison of grain growth characteristics and film properties of copper films formed by various methods [Faculty of Engineering, Kansai Univ., *Kobe Advanced ICT Research center, NICT] Y. Harada, H. Tanaka* and S. Shingubara

<CMP>

(5-14) Evaluation of MBT Anticorrosive Layer on Cu Surface for Chemical-Mechanical Polishing Application [Dept. of Physical Electronics, Tokyo Institute of Technology, *Dept. of Electrical, Electronics and Computer Engineering, Chiba Institute of Technology, **Nitta Haas Incorporated] H. Nishizawa, O. Sugiura*, Y. Matsumura** and M. Kinoshita**

(5-15) Surface Roughness Performance of Electro Chemical Mechanical Polishing (ECMP) [Ebara Research Co., Ltd., Ebara Corp.] Y. Toma, A. Kodera, T. Suzuki, T. Saitoh, H. Hiyama, I. Kobata, Y. Wada*, A. Fukunaga* and M. Tsujimura*

(5-16) Study on groove pattern layout for slurry flow control in CMP process [Dept. of Mechanical Information Science and Technology, Kyushu Institute of Technology] K. Kimura, K. Nagayama, H. Morishita, Y. Inatsu, P. Khajornrungruang

(5-17) Characterization of Organic Dielectric for Sealing Air-Gaps with STP Technology [NTT, *NTT-AT, **Sumitomo Bakelite Co., Ltd., ***Dainippon Screen Mfg. Co., Ltd.] N. Sato, K. Machida*, H. Ishii, Y. Ishimura**, H. Saito**, S. Asakuma**, M. Kawagoe*** and H. Adachi***

(5-18) Characteristics of Thick Multilevel Interconnection Based on Gold Electroplating and STP Technique [NTT Microsystem Integration Laboratories, NTT Corp., *NTT Advanced Technology Corp.] N. Shimoyama, K. Ono, N. Sato, H. Ishii, T. Kamei*, K. Kudou* and K. Machida*

<Packaging/Characterization>

(5-19) Nanometer-Scale Stress Field Evalluation of Cu/ILD Pattern; Comparison between Cathodoluminescence Spectroscopy and Thermal Stress Analyses by Finite Element Method [Process&Manufacturing Engineering Center, Toshiba Co, *Photonic Frontier Project, R&D Center, HORIBA, Ltd., **Ceramic Physics Laboratory & Research Institute for Nanoscience, Kyoto Institute of Tech.] M. Kodera, S. Ito, M. Hasunuma, S. Kakinuma* and G. Pezzotti**

(5-20) Low-k materials face damages induced by mismatch of thermal expansion around the global bus lines when operation frequency is high [Univ. of Yamanashi] H. Kato, T. Yoshida, T. Tatsuta and E. Kondoh

(5-21) Mass Production of Wafer-Level-Packaging Technology using Silicon-Via-Contacts For Optical And Other Sensor Applications [SCHOTT Advanced Packaging Singapore Ltd., *NEC SCHOTT Components Corp.] J. Leib, H. Yamamoto*

<Reliability>

(5-22) Cu/Low-k TDDB Degradation Using Ultra Low-k (ULK) Dielectrics [Renesas Technology Corp., *Renesas Semiconductor Engineering Corp.] N. Miura, K. Goto, S. Hashii*, N. Suzumura, H. Miyazaki, M. Matsumoto, M. Matsuura and K. Asai

(5-23) The Stress Control of Capping Insulators as a Key to Preventing Electromigration and Stress-Induced Voiding Failures [Process Development Dept., Renesas Technology Corp.] D. Kodama, S. Fukui, N. Miura, K. Goto, N. Suzumura, M. Matsuura, T. Furusawa and H. Miyazaki

<Silicide>

(5-24) Anomalous Whisker Generation in Ni-Silicided Source and Drain for Three-Dimensional Beam-Channel MOS Transistor on SOI Substrate [Research Center for Nanodevices and Systems, Hiroshima Univ.] S. Matsumura, A. Sugimura, K. Okuyama and H. Sunami

(5-25) Low-resistance Ti-silicide contact formation to p+ layer for use in analog devices [New Japan Radio Co., Ltd.] H. Kuchiji and M. Sato

(5-26) Properties of chemical reaction during Ni and Ni-silicide deposition using Ni $(PF3)_4$ and Si_3H_8 [Tri Chemical Laboratories Inc., *Meiji Univ., **Toyota Technological Institute] M. Ishikawa*, I. Muramoto, H. Machida, S. Imai*, A. Ogura*, Y. Ohshita**

[Sep. 27, 2006]

Session 6 **Low-k (2)** Chairperson: E. Kondoh, T. Tamaru

9:30 – 9:55(**6-1**) **Invited:** Interface Characterization and Properties for Future Generation Interconnect Technologies [Stanford Univ.] R. H. Dauskardt

9:55 – 10:15(**6-2**) Material design of porous low-k materials for 45 nm node interconnects [Process & Manufacturing Engineering Center, Semiconductor Company, Toshiba Corp., *Advanced CMOS Technology Dept., SoC R&D Center, Semiconductor Co, Toshiba Corp., **Semiconductor Technology Development Group, Semiconductor Business Unit, Sony Corp.] K. Watanabe, H. Miyajima, M. Shimada, T. Sakanaka, N. Nakamura*, T. Shimayama**, Y. Enomoto**, H. Yano and T. Yoda

10:15 – 10:35(**6-3**) Stress analysis of low-k material interface during CMP [Ebara Research Co., Ltd., *Toshiba Corp., **P Ebara Corp.] Y. Mochizuki*, H. Shibata*, M. Tsujimura** and H. Hiyama

10:35 – 10:55(**6-4**) The Optimization of Porous Organosilicate Glasses Produced by Plasma-Enhanced Chemical Vapor Deposition [Air Products and Chemicals, Inc.] M.L. O'Neill, R.N. Vrtis, M.K. Haas, S.J. Weigel, D.J Wu, P.T. Hurley, S.G. Mayorga, M.D. Bitner, D. Sinatore and S. Motika

10:55 – 11:15(**6-5**) Si-C_2H_4-Si network formation for improvement of PECVD SiOCH film properties [Taiyo Nippon Sanso Corp., *First Principles Simulation Group, Computational Materials Science Center, National Institute for Materials Science, **The FSIS Center for Collaborative Research, Institute of Industrial Science, Univ. of Tokyo, ***Semiconductor Leading Edge Technologies, Inc.] M. Shinriki, N. Tajima*, T. Hamada**, T. Ohno*, K. Yoneda***, S. Kondo***, S. Ogawa***, K. Miyazawa, Y. Inaishi, K. Sakoda, S. Hasaka and M. Inoue

11:15 – 11:30 Break

Session 7 **Contact / Silicide** Chairperson: H. Machida

11:30 – 11:50(**7-1**) New barrier metal and ALD-W process for low stable resistance in contact metallization beyond 45-nm CMOS [Renesas Techology Corp.] K. Ichinose, A. Yutani, K. Maekawa, K. Asai and M. Yoneda

11:50 – 12:10(**7-2**) Native oxide removal application using NF3/NH3 remote plasma for Ni Silicide process [Applied Materials Japan, * Applied Materials, **Renesas Technology Corp.] T. Kuratomi, K. Tanaka, D. Diehl, S-E. Phan*, X. Lu*, D. Or*, J. Lei*, G. Lai*, K. Lavu*, C. Jiang*, K. Moraes*, C-T. Kao*, T. Futase** and K. Maekawa**

12:10- 12:30(**7-3**) Evaluation of very low resistivity TiNx film using Cat (catalytic) radical reaction with $TiCl_4$ [Institute For Semiconductor Technologies ULVAC, Inc., *Semiconductor Equipment Div.1 ULVAC, Inc.] M.Harada, K.Kamada, S.Toyoda, N.Katou*, H.Ushikwa*

12:30 – 13:30 Lunch

Session 8 **Packaging / Emerging Technology** Chairperson: Owada

13:30 – 13:55(**8-1**) **Invited:** Carbon nanotube interconnect technologies [Fujitsu Laboratories Ltd. and MIRAI-Selete] Y. Awano

13:55 – 14:15(**8-2**) Damageless Chip Stacking Using Compliant Bumps [Applied Electronics Research Center, Kumamoto Technology and Industry Foundation, *Faculty of Information Science and Electrical Engineering, Kyushu Univ.] N. Watanabe and T. Asano*

14:15 – 14:35(**8-3**) Low-Cost Through-hole Electrodes Interconnection for 3D-SiP Using Room-temperature Bonding [Mechanical Engineering Research Laboratory, Hitachi, Ltd., *Renesas Technology Corp.] N. Tanaka, Y. Yoshimura, T. Naito* and T. Akazawa*

14:35 – 14:55(**8-4**) On-Chip Differential-Transmission-Line (DTL) Interconnect for 22nm Technology [Integrated Research Institute, Tokyo Institute of Technology] K. Okada, H. Ito and K. Masu

14:55 – 15:15(**8-5**) A Crackless and High Reliable Cu eTrim Fuse using the Pinch Effect for 65nm [Process Development Dept., Renesas Technology Corp.] K. Kono, T. Yonezu, S. Obayashi, M. Arakawa, Y. Asano, T. Uchida and T. Iwamoto

15:15 – 15:30 Break

Session 9 **Integration** Chairperson: S. Kondo, F. Ito

15:30 – 15:55(**9-1**) **Invited:** Low Damage Process of Extreme Low-k Dielectrics Integration for 45nm Generation and Beyond [Taiwan Semiconductor Manufacturing Company, Ltd.] C-H Hsieh, C.L. Huang, M.C. Liang, T.L. Lee, J.J. Lee, B.C. Perng, K.C. Lin, S.L. Shue, C.H. Yu and M.S. Liang

15:55 – 16:15(**9-2**) High Performance Ultra Low-k (k=2.0/keff=2.4) Hybrid Dielectrics / Cu Dual-Damascene Interconnects with Selective Barrier Layer for 32 nm-node [Center for Semiconductor Research & Development, Semiconductor Company, Toshiba Corp., *Process & Manufacturing Engineering Center, Semiconductor Company, Toshiba Corp.] Y. Hayashi, K. Tsumura, M. Shimada*, K. Watanabe*, H. Miyajima*, T. Usui and H. Shibata

16:15 – 16:35(**9-3**) Low-k/Cu Interconnect Integration with Low-Damage Ash Using Atomic Hydrogen [Semiconductor Leading Edge Technologies, Inc.] K. Tomioka, S. Kondo, N. Ohhashi, T. Suzuki, E. Soda and N. Kobayashi

16:35 – 16:55(**9-4**) Barrier-free interconnect with organic spin-on dielectric [Consortium for Advanced Semiconductor Materials and Related Technologies (CASMAT), *Sumitomo Bakelite Co., Ltd.] N. Maeda, Y. Takimoto, K. Maejima*, M. Nakajima* and K. Funatsu

16:55 – 17:15(**9-5**) PECVD Ultra Low K material appropriate to the “post-integration porogen removal approach” [STMicroelectronics, * CEA-LETI] L. Favennec, V. Jousseaume*, A. Zenasni*, M. Assous*, T. David* and G. Passemard

17:15 – 17:35(**9-6**) Silylation Gas Restoration Subsequent to All-in-one RIE Process without Air Exposure for Porous Low-k SiOC/Copper Dual-Damascene Interconnects [Process & Manufacturing Engineering Center, Semiconductor Co, Toshiba Corp., *Center for Semiconductor R&D, Advanced BEOL Technology Dept., Semiconductor Co, Toshiba Corp., **Fundamental Process Group, R&D Division, Tokyo Electron AT Ltd., ***Leading Edge Process Development Center, Tokyo Electron Ltd.] A. Kojima, N. Nakamura*, N. Matsunaga*, H. Hayashi, K. Kubota**, R. Asako***, K. Maekawa***, H. Shibata*, T. Yoda and T. Ohiwa

17:35 – 17:45 **Closing Remarks** S. Shingubara [Kansai Univ.]