# ADMETA 2005 PROGRAM

## Advanced Metallization Conference 2005: 15th Asian Session

Conference: Oct. 13-14, 2005 Sanjo Conference Hall, The Univ. of Tokyo, Tokyo

**【Oct. 13, 2005】**

**Session 1 Opening Session** Chairperson: K. Masu

9:50 - 10:05 Opening Remarks, M. Tsujimura, Chair of Asian Session [Ebara Corp.]
Formal Greetings, H. Komiyama [The Univ. of Tokyo]
Award Presenting Ceremony

10:05 – 10:35**(1-1)** **Keynotes:** A New Smart-Stack Technology for Three-Dimensional LSI [Dept. of Bioengineering and Robotics, Tohoku Univ.] M. Koyanagi

10:35 – 11:05**(1-2)** **Keynotes:** Advanced BEOL R&D activity at Crolles Alliance [ST Microelectronics] J. Torres

**Session 2 Low-k (1)** Chairperson: T. Yoda

11:05 – 11:30**(2-1)** **Invited:** Interconnect Technology Featuring ULK Stacked Hybrid Structures [Semiconductor Technology Development Group, Semiconductor Solutions Network Co., Sony Corp.] T. Hasegawa, Y. Enomoto

11:30 – 11:50**(2-2)** Improvement of Mechanical Properties of Porous SiOCH films by Post-cure Treatments [System Devices Research Laboratories, NEC Corp.] F. Ito, T. Takeuchi and Y. Hayashi

11:50 – 12:10**(2-3)** Film Characterization and Integration of UV Cured Ultra Low-k for 45nm Node Cu/Low-k Interconnects [Renesas Technology Corp., *Renesas Semiconductor Engineering Corp., **ASM Japan K.K.] K. Goto, S. Hashii*, M. Matsumoto, N. Miura, T. Furusawa, M. Matsuura, A. Ohsaki, N. Ohara**, N. Tsuji** and K. Matsushita**

**12:10 – 13:10 Lunch**

**Session 3 Low-k (2) / NiSi** Chairperson: H. Machida

13:10 – 13:35**(3-1)** **Invited:** Advanced Electronic Materials for ULSI Metallization [Dow Chemical Co.] M. E. Mills, Y. Ida and K. Ohba

13:35 – 13:55**(3-2)** Effects of UV-cure Time on Electrical Properties of Cu/Porous SiOC Interconnects [Semiconductor Leading Edge Technologies, Inc. (Selete), *ASM Japan K.K] M. Kato, K. Yoneda, S. Nakao, S. Kondo, N. Kobayashi, N.Matsuki*, K. Matsushita*, N. Ohara*, A. Fukazawa*, T. Ikegawa* and T. Kimura*

13:55 – 14:15**(3-3)** Material design of balance between high mechanical strength and high plasma resistance for porous PE-CVD SiOC film (k=2.3) [Process and Manufacturing Engineering Center, Semiconductor Co., Toshiba Corp., *Semiconductor Technology Development Div., Semiconductor Solutions Network Co., Sony Corp.] H. Miyajima, H. Masuda, T. Idaka, T. Shimayama*, Y. Kagawa*, K. Tabuchi*, H. Yano, T. Hasegawa*, S. Kadomura* and T. Yoda

14:15 – 14:35**(3-4)** Study of Pt Addition to Solve NiSi Integration Issues on CMOS Devices [Central Research and Development Div., United Microelectronics Corp.] Y. Y. Chiang, Y. L. Chang, T. Y. Hung, Y. W. Chen, K. Shieh, C. C. Huang and S. F. Tzou

14:35 – 14:55**(3-5)** Impact of Fluorine Ion Implantation on Narrow Line Effect of Nickel Silicide [Process Development Dept., Process Technology Development Div., Production and Technology Unit, Renesas Technology Corp.] T. Yamaguchi, K. Kashihara, T. Okudaira, T. Kosugi, H. Miyatake and M. Yoneda

14:55 – 15:15**(3-6)** Chemical Vapor Deposition of Ni-silicide for Gate Electrodes [Business development, Tri Chemical Laboratories Inc., *Meiji Univ., **Toyota Technological Institute] M. Ishikawa, I. Muramoto, H. Machida, S. Imai*, A. Ogura*, Y. Ohshita**

**15:15 – 15:35 Coffee Break**

**Session 4 Metallization** Chairperson: S. Shingubara

15:35 – 16:00**(4-1)** **Invited:** Electroless Deposition of Co-based Alloys for Selective Capping Applications [Freescale Semiconductor, Inc.] L. M. Michaelson, V. Mathew, M. Gall, M. Hauschildt, E. Acosta, S. Garcia

16:00 – 16:20**(4-2)** Countermeasure against Selectivity Loss of W metallic Cap in Cu Interconnects [Micro Device Div., Hitachi, Ltd.] H. Ashihara, K. Ishikawa and T. Saito

16:20 – 16:40**(4-3)** Evaluation of liquid additives as reducing agent and entrainer for supercritical fluid deposition of copper using in situ monitoring [Department of Materials Engineering, The Univ. of Tokyo, *Department of Electronic Engineering, The Univ. of Tokyo] T. Momose, T. Ohkubo, M. Sugiyama* and Y. Shimogaki

16:40 – 17:00**(4-4)** Influence of Cu Electroplating Solutions on Leakage Current in Self-Assembled Porous Silica Low-k Films [MIRAI-ASET, *MIRAI-ASRC, AIST, **RCNS, Hiroshima Univ.,] M. Shimoyama, R. Yagi, S. Chikaki, N. Fujii, T. Nakayama, K. Kohmura, H. Tanaka, K. Kinoshita and T. Kikkawa*,**

17:00 – 17:20**(4-5)** Cu plating under high resistance Cu seed increased by scattering effect [Ebara Corp.] M. Hodai, T. Nakada and M. Tsujimura

17:20 – 17:40**(4-6)** Innovative Al Damascene Process for Nanoscale Interconnects [Process Development Team, Semiconductor R&D Center, Samsung Electronics Co. Ltd.] K. I. Choi, S. H. Han, S. Y, D.-Y Kim, J. W. Hong, S. W. Lee, B. H. Kim, S.-T Kim, U. I. Chung and J. T. Moon

17:40 – 18:00**(4-7)** **Guest Paper from USA** [Dow Chemical Co.] M. E. Mills

**18:10 – 20:00 Banquet**

**【Oct. 14, 2005】**

**Session 5 Copper Surface Treatment** Chairperson: K. Kinoshita

9:30 – 9:55**(5-1)** **Invited:** Single Wafer Cleaning Process on Next Generation device [Samsung Electronics Co., Ltd] C. Hong

9:55 – 10:15**(5-2)** Novel Cu Surface Cleaning Technology Using Extremely Low Oxygen Pressure [National Institute of Advanced Industrial Science and Technology (AIST)] K. Endo, N. Shirakawa, Y. Yoshida, S. I. Ieda, T. Mino, E. Gofuku and E. Suzuki

10:15 – 10:35**(5-3)** Low Temperature Dry Cleaning Technology using Formic Acid in Cu/low-k Multilevel Interconnects for 45 nm node and beyond [Akiruno Technology Center, Fujitsu Limited] J. Nakahira, K. Ishikawa, N. Nishikawa, M. Hayashi, A. Asmeil, Y. Nakata, Y. Mizushima, H. Kudo, T. Kurahashi, Y. Mishima Y. Takigawa, M. Nakaishi and K. Watanabe

10:35 – 10:55**(5-4)** Hot Filament Technology for Quick and Low Temperature Copper Surface Recuperation [Univ. of Yamanashi] E. Kondoh

10:55 – 11:10 Break

**Session 6 Integration** Chairperson: S. Kondo

11:10 – 11:35**(6-1)** **Invited:** BEOL Process Integration with Cu/SiCOH (k=2.8) Low-k Interconnects at 65 nm Groundrules [IBM Corp.] S. L. Lane

11:35 – 11:55**(6-2)** High-Density Differential Transmission Line Bus Structure for Future Subnanometer Technologies [Precision and Intelligence Laboratory, Tokyo Institute of Technology] M. Kimura, H. Ito, H. Sugita, K. Okada and K. Masu

11:55 – 12:15**(6-3)** Nanometer-Scale Stress Detection of Patterned ILD Using Cathodoluminescence Piezo-Spectroscopic Assessments in a Nano-Stress Microscope [Process & Manufacturing Engineering Center, Toshiba Co., *Photonic Frontier Project, R&D Center, HORIBA,Ltd., **Precision Machinery Co., Ebara Corp., ***Ceramic Physics Laboratory & Research Institute for Nanoscience, Kyoto Institute of Technology] M. Kodera, S. Kakinuma*, Y. Saijo*, M. Tsujimura** and G. Pezzotti***

**12:15 – 13:05 Lunch**

**13:05 – 14:25 Session 7 Poster Session**

<Low-k>

(7-1) Characterization of Annealing SiOC Films [Toray Research Center, Inc.] K. Matsuda, R. Miyoshi, H. Seki, M. Takeda, K. Inoue, T. Ajioka, R. Sugie, T. Matsunobe, H. Hashimoto and M. Yoshikawa

(7-2) A method of forming Si-$CH_2$ in low-k SiC barrier dielectrics using BTMSA (Bis-trimethylsilylacetylene) [Japan Advanced Chemicals, *National Institute of Advanced Industrial Science and Technology (AIST)] S. Yasuhara and K. Endo*

<Metallization>

(7-3) Nucleation behavior of CVD Cu on Ru substrate having different crystal orientation [Department of Materials Engineering, The Univ. of Tokyo, *Div. of Univ. Corporate Relations, The Univ. of Tokyo, **Technology

Development Center, Tokyo Electron AT Limited] H. Kim, T. Koseki, T. Ohba*, T. Ohta*, Y. Kojima**, H. Sato**, N. Yoshii** and Y. Shimogaki

(7-4) Effects of the adding small amounts of Ag on Cu metallization [Department of Materials Engineering, The Univ. of Tokyo] B. Zhao, H. Kim, M. Tsutsumi, T. Koseki and Y. Shimogaki

(7-5) High-performance Copper Plating Process for 65nm and 45nm Technology Nodes [Applied Materials, Inc., *Enthone, Inc.,] Y.-C. Huang, X. Lin*, B. Zheng, C. Ngai, V. Paneccasio*, J. Behnke, C. Witt*, J. Dukovic, A. Rosenfeld

(7-6) Evaluation of MOSFET Characteristics with Thick Interconnection Formed by Gold Electroplating for Seamless Integration Technology [NTT Microsystem Integration Laboratories, NTT Corp., *NTT Advanced Technology Corp., **Shimane Univ.] N. Shimoyama, H. Ishii, N. Sato, T. Kamei*, K. Kudou*, M. Yano*, Y. Okazaki, T. Tsuchiya** and K. Machida

(7-7) Influence of Copper Plating and Die Layout on the Copper CMP Performance [IMEC, *ASM NuTool Inc., **ASM Belgium N.V.] I. Vos, N. Heylen, J. L. Hernandez, T. Wang*, T. Truong*, B. Basol*, H. Sprey** and S. Vanhaelemeersch

(7-8) An experimental study of atomic layer deposited films on dielectric substrates with different porosity [IMEC, *Unité POLY, UCL] Y. Travaly, J. Schuhmacher, G. Mannaert, M. R. Baklanov, S. Giangrandi, O. Richard, B. Brijs, M. V. Hove, A. M. Jonas*, K. Maex

(7-9) Application of ultrathin VN barrier between Cu interconnects and SiOC layer [Department of Electrical and Electronic Engineering, Kitami Institute of Technology, *Institute for Materials Research, Tohoku Univ.] M. B. Takeyama, G. Mizuno, E. Aoyagi*, A. Noya

(7-10) High Purity Ruthenium Thin Films Depositions Using a $RuO_4$ Solvent Solution [Air Liquide Laboratories] J. Gatineau, K. Yanagita, C. Dussarrat

(7-11) Characterization of Electroless Ni Alloy Film as a Diffusion Barrier and Capping Layer on Low-k Inter-level-Dielectrics [Waseda Univ.] M. Yoshino, T. Masuda, S. Wakatsuki, J. Sasano, I. Matsuda, Y. S.-Diamand, T. Osaka

(7-12) Effect of the combination of PEG and HIQSA additives on electroless copper deposition for ULSI interconnection [Waseda Univ.] M. Hasegawa, T. Nakanishi, Y. Okinaka, Y. S.-Diamand, T. Osaka

(7-13) Integration of porous Ultra Low K material with ALD metallic barrier [CEA-LETI D2NT, *ST Microelectronics (Crolles2), **Philips Semiconductors Crolles R&D] S. Maîtrejean, X. Houziaux*, M. Fayolle, W. Besling**, H. Feldis, V. Jousseaume, G. Passemard*

(7-14) Copper Line Resistance Behavior in Pd-activated Co Alloy Capping Process [Precision Machinery Co., Ebara Corp., *Semiconductor Leading Edge Technology, Inc.] X. Wang, A. Owatari, T. Ishibashi, D. Takagi, J. Tsujino, T. Koba, T. Ishigami*, S. Kondo* and N. Kobayashi*

(7-15) Epitaxial $NiSi_2$ layers with extremely flat interfaces in Ni/Ti/Si(001) system [Graduate School of Engineering, *EcoTopia Science Institute, **CCRAST, Nagoya Univ.] A. Suzuki, K. Okubo, O. Nakatsuka*, A. Sakai, M. Ogawa** and S. Zaima

(7-16) To Transfer Familiar Dry-Process Design to Supercritical Fluid Chemical Deposition Apparatus for Studying Deposition Science [Interdisciplinary Graduate School of Medicine and Engineering, Univ. of Yamanashi] E. Kondoh and J. Fukuda

(7-17) Barrier properties of extremely thin ZrN films in Cu/SiOC system [Department of Electrical and Electronic Engineering, Kitami Institute of Technology] M. B. Takeyama, M. Sato and A. Noya

<CMP>

(7-18) An Analysis of Copper Surface Layers for Chemical Mechanical Poising Process with Spectroscopic Ellipsometry [Department of Physical Electronics, Tokyo Institute of Technology, *Department of Electrical, Electronics and Computer Engineering, Chiba Institute of Technology, **Nitta Haas Incorporated] H. Nishizawa, O. Sugiura*, Y. Matsumura**, S Haba** and M. Hanazono**

(7-19) Effect of pH on Polymer abrasive Cu-CMP slurries [Electronic & Engineered Materials Laboratory, Mitsui Chemicals, Inc., *Functional Polymeric Materials Laboratory, Mitsui Chemicals, Inc.] S. Nakamura, K. Shindo, S. Fujii, A. Eto* and T. Ishizuka*

(7-20) Finite element analysis of the stress in vias with Cu/Low-k structure [Ebara Research Co., *Toshiba Corp., **Ebara Corp.] Y. Mochizuki, H. Shibata*, M. Tsujimura**, H. Hiyama

(7-21) The Advanced CMP "$mC^2$" for Cu/Low-k Planarization Technology [Ebara Corp.] Y. Wada, T. Kohama, H. Nagano, K. Tokushige, A. Fukunaga, M. Tsujimura

<Integration>

(7-22) Dual damascene for mation for 45nm-node and beyond [Tokyo Electron Ltd., *Tokyo Electron AT Ltd., **JSR Corp., ***Ebara Corp.] K. Maekawa , H. Nagai , M. Iwashita* , M. Muramatsu* , K. Kubota* , K. Hinata* , T. Kokubo** , A. Shiota** , M. Hattori**, H. Nagano***, K. Tokushige***, M. Kodera***, K. Mishima***

(7-23) Characteristics of Film Peel-off in STP Technology [NTT Advanced Technology, *NTT Microsystem Integration Laboratories, **Dainippon Screen MFG] T. Kamei, N. Sato*, K. Kudou, M. Kawagoe**, H. Adachi** and K. Machida*

(7-24) High Frequency Characterization of Copper/Low-k Interconnects with Feature Size Scaling [*A*STAR Institute of Microelectronics, **School of Electrical and Electronic Engineering, Nanyang Technological Univ.] R. Kumar*·**, T. K. S. Wong**, B. Ramanamurthy* and S. C. Rustagi*

(7-25) How to deliver a high-frequency clock over than 100GHz using Common BEOL Technologies [Interdisciplinary Graduate School of Medicine and Engineering, Univ. of Yamanashi, *Tomakomai National Colledge of Technology] H. Kato, T. Kohori, K. Watanabe, Y. Kodaira, E. Kondoh, T. Akitsu and H. Kato*

(7-26) STP Transfer System for Uniform Dielectrics Formation [Dainippon Screen MFG. Co. Ltd., *NTT] M. Kawagoe, T. Komura, T. Yanagida, H. Adachi, N. Sato* and K. Machida*

(7-27) Suppression of Defects in ArF Lithography with Pre-Treatment for Cu/low-k Interconnect [Consortium for Advanced Semiconductor Materials and Related Technologies (CASMAT)] H. Nakao, T. Narita, T. Hasebe, H. Tonokawa and K. Yanai

<Copper Surface Treatment>

(7-28) Low-Damage Ashing by Atomic Hydrogen for Porous Low-k/Cu Interconnects [Semiconductor Leading Edge Technologies, Inc., *Graduate School of Engineering Science, Osaka Univ.] K. Tomioka, E. Soda, N. Kobayashi, K. Mochidzuki*, M. Takata*, S. Uda*, Y. Yuba* and Y. Akasaka*

(7-29) Robustness Enhancement for Subsequent Plasma Damages Utilizing Surface Modification Layer Induced by He Plasma [Consortium for Advanced Semiconductor Materials and Related Technologies (CASMAT)] K. Yanai, T. Hasebe, K. Sumiya, S. Oguni and K. Koga

(7-30) A Study of Plasma Treatments Limiting Metal Barrier Diffusion into Porous Low-k Materials [CEA/LETI, *ST Microelectronics Central R&D, **CNRS/LTM] T. David, N. Posseme*, T. Chevolleau**, M. Darnon**, O. Louveau*, D. Louis, G. Passemard* and O. Joubert**

**Session 8 Reliability** Chairperson: N. Shimizu

14:25 – 14:50**(8-1)** **Invited:** Self-Forming Barrier Process with Mn addition in Cu Metallization [*Dept. of Materials Science, Tohoku Univ., STARC] J. Koike*, M. Wada*, T. Usui, H. Nasu, S. Takahashi, N. Shimizu, T. Nishikawa, M. Yoshimaru and H. Shibata

14:50 – 15:10**(8-2)** New Reliability Failure by Water Absorption into Low-k SiOCH Dielectric on Cu Dual-damascene Interconnects [SoC Research & Development Center, Semiconductor Co., Toshiba Corp., *Process & Manufacturing Engineering Center, Semiconductor Co., Toshiba Corp.] K. Tsumura, H. Miyajima*, S. Ito*, T. Usui and H. Shibata

15:10 – 15:30**(8-3)** Impact of damage restoration process on electrical properties and reliability of porous low-k SiOC/Copper dual-damascene interconnects [Advancd CMOS Technology Department, Soc R&D Center, Semiconductor Co., Toshiba Corp., *Process & Manufacturing Engineering Center, Semiconductor Co., Toshiba Corp., **Semiconductor Technology Development Group, Semiconductor Solutions Network Co., Sony Corp.] N.Nakamura, N.Yamada*, S.Nakao*, K. Akiyama*, H.Miyajima*, N.Matsunaga, Y.Enomoto** and H.Shibata

15:30 – 15:50**(8-4)** Thermal dependence of leakage pathways in Cu/ULK advanced interconnects [*CEA-DRT - LETI/DTS - CEA/GRE, **ST Microelectronics] C. Guedj*, V. Arnal**, M. Aimadeddine**, J.F. Guillaumond*·**, L. Arnaud*, J. P. Barnes*, L. L. Chapelon**, G. Reimbold*, J. Torres**, G. Passemard** and F. Boulanger*

15:50 – 16:10**(8-5)** Thorough thermal stress characterization of Cu film for high highly reliable sub-100nm interconnect [Unit Process Technology Department, Process Development Div., Semiconductor Technology Development Group, Semiconductor Solution Network Co., Sony Corp.] T. Fukuura, N. Komai, K. Inoue and R. Kanamura

**16:10 – 16:30 Break**

**Session 9 Low-k(3)** Chairperson: T. Tamaru

16:30 – 16:50**(9-1)** Improvement of the electrical performance of Cu / Aurora® ULK interconnects using an advanced BEOL integration

scheme [IMEC, *Matsushita Electric Industrial Co., Ltd., **ASM Belgium, ***ASM Japan K.K.] Y. Travaly, A. Ikeda*, Z. Tőkei, D. Hendrickx, J. V. Aelst, L. Carbonell, H. Struyf, Y. –L. Li, N. Kemeling***, A. Fukazawa***, N. Matsuki***, F. Iacopi, H. Sprey**, G. Beyer and M. V. Hove

16:50 – 17:10**(9-2)** Mechanical-property Improvement for PECVD SiOCH Film by Hydrocarbon Substitution Effect using Molecular Modeling [Taiyo Nippon Sanso Corp., *First Principles Simulation Group, Computational Materials Science Center, National Institute for Materials Science, **The FSIS Center for Collaborative Research, Institute of Industrial Science, The Univ. of Tokyo, ***Research Dept.1, Semiconductor Leading Edge Technologies, Inc. (Selete)] M. Shinriki, N. Tajima*, T. Hamada**, T. Ohno*, N. Kobayashi***, S. Hasaka and M. Inoue

17:10 – 17:30**(9-3)** Overcoming porous ULK integration issues by using post integration porogen removal approach [CEA-LETI, *Rohm and Haas Electronic Materials, **ST Microelectronics] M. Fayolle, M. Assous, S. Maitrejean, T. David, V. Jousseaume, H. Trouvé*, G. Passemard**

17:30 – 17:50**(9-4)** Film property of spin-on barrier dielectric [Consortium for Advanced Semiconductor Materials and Related Technologies (CASMAT), *Sumitomo Bakelite Co., Ltd.] N. Maeda, S. Arase, Y. Homma, H. Saito*, K. Maejima* and I. Kato

**17:50 – 18:00 Closing Remarks** A. Ohsaki [Renesas Technology Corp.]